This listing of claims will replace all prior versions, and listings, of claims in the present application.

LISTING OF CLAIMS

Claim 1 (Previously Presented) A bipolar transistor comprising:

a semiconductor substrate layer;

a conductive back electrode located over the semiconductor substrate layer for receiving a bias voltage;

an insulating layer located directly over said conductive back electrode;

a first semiconductor layer located over said insulating layer, wherein said first semiconductor layer comprises a base which includes a first conductive type dopant and an extrinsic collector which includes a second conductivity type dopant, said extrinsic collector borders said base, and said base is electrically isolated from said conductive back electrode; and

an emitter comprising a second semiconductor layer of the second conductivity type dopant located over a portion of said base, wherein said conductive back electrode is biased to form an inversion charge layer at a bottom portion of said base region at an interface between said first semiconductor layer and said insulating layer and said inversion charge layer serves as an intrinsic collector of said transistor.

Claim 2 (Previously Presented) The bipolar transistor of Claim 1 wherein a portion of said base is doped to form an extrinsic base.

Claim 3 (Original) The bipolar transistor of Claim 2 wherein the extrinsic base, the emitter, the extrinsic collector and the exposed surfaces of the conductive back electrode each include a silicide.

Claim 4 (Original) The bipolar transistor of Claim 3 wherein the silicide is in contact with a metal contact that is located atop the silicide inside a contact opening formed in an interconnect dielectric.

Claim 5 (Original) The bipolar transistor of Claim 1 wherein the emitter comprises a single-finger.

Claim 6 (Original) The bipolar transistor of Claim 1 wherein the emitter comprises multi-fingers.

Claim 7 (Original) The bipolar transistor of Claim 2 wherein the extrinsic collector and the extrinsic base are raised regions.

Claim 8 (Original) The bipolar transistor of Claim 1 wherein a spacer is located on sidewalls of the emitter.

Claim 9 (Original) The bipolar transistor of Claim 1 wherein said insulating layer is a thin insulating layer having a thickness from about 1 to about 15 nm.

Claim 10 (Original) The bipolar transistor of Claim 9 wherein another insulating layer that is thicker than the thin insulating layer is located adjacent thereto, said another insulating layer is a buried oxide of a silicon-on-insulator.

Claim 11 (Original) The bipolar transistor of Claim 2 wherein the base contains a p-type dopant, the emitter contains an n-type dopant, the extrinsic collector contains an n-type dopant and the extrinsic base contains a p-type dopant.

Claim 12 (Original) The bipolar transistor of Claim 2 wherein the extrinsic base diffuses minimally into the base so as not to be in contact with the underlying insulating layer.

Claim 13 (Previously Presented) An integrated semiconductor structure comprising:

a bipolar transistor comprising a conductive back electrode for receiving a bias voltage;

an insulating layer located over said conductive back electrode;

a first semiconductor layer located over said insulating layer, wherein said first semiconductor layer comprises a base which includes a first conductive type dopant and an extrinsic collector which includes a second conductivity type dopant, said extrinsic collector borders said base, and said base is electrically isolated from said conductive back electrode;

an emitter comprising a second semiconductor layer of the second conductivity type dopant located over a portion of said base region, wherein said conductive back electrode is biased to form an inversion charge layer at a bottom portion of said base region at an interface between said first semiconductor layer and said insulating layer and said inversion charge layer serves as an intrinsic collector of said transistor; and

at least one adjacent complementary metal oxide semiconductor device, said bipolar transistor and said at least one adjacent complementary metal oxide semiconductor device are separated by an isolation region.

Claim 14 (Original) The integrated semiconductor structure of Claim 13 wherein the complementary metal oxide semiconductor device is a field effect transistor.

Claims 15-31 (Cancelled)

Claim 32. (New) A circuit comprising:

a voltage source for applying a bias voltage of less than or equal to 3 V;

a current source; and

a collector-less bipolar junction transistor on a silicon-on-insulator substrate comprising an emitter, a base region, and a back gate-induced minority carrier inversion layer which is an inversion charge layer,

wherein said voltage source is electrically coupled to said silicon-on-insulator substrate to apply said bias to maintain said inversion charge layer at a bottom of said base region, and wherein said inversion layer is an intrinsic collector of said collector-less bipolar junction transistor.

Claim 33. (New) The circuit of Claim 32, wherein said collector-less bipolar junction transistor comprises:

a conductive back electrode for receiving said bias voltage;

an insulating layer located over said conductive back electrode;

a first semiconductor layer located over said insulating layer and comprising said base region having a doping of a first conductive type and an extrinsic collector having a doping of a second conductivity type and bordering said base region; and

said emitter comprising a second semiconductor layer has a doping of said second conductivity type and is located over a portion of said base region,

wherein said conductive back electrode is biased to form said inversion charge layer in said base region at an interface between said first semiconductor layer and said insulating layer.

Claim 34 (New) A method of operating a circuit comprising:

applying a bias voltage of less than or equal to 3 V to a substrate of a collector-less bipolar transistor located on a silicon-on-insulator substrate; and

applying a current to a base contact of said bipolar transistor,

wherein said collector-less bipolar junction transistor comprises an emitter, a base region, and a back gate-induced minority carrier inversion layer which is an inversion charge layer, and wherein said inversion layer is an intrinsic collector of said collector-less bipolar junction transistor that is formed only when said silicon-on-insulator substrate is biased, wherein said bias voltage maintains said inversion charge layer at a bottom of said base region.

Claim 35 (New) The method of Claim 34, wherein said collector-less bipolar junction transistor comprises:

a conductive back electrode for receiving said bias voltage;

an insulating layer located over said conductive back electrode;

a first semiconductor layer located over said insulating layer and comprising said base region having a doping of a first conductive type and an extrinsic collector having a doping of a second conductivity type and bordering said base region; and

said emitter comprising a second semiconductor layer has a doping of said second conductivity type and is located over a portion of said base region,

wherein said conductive back electrode is biased to form said inversion charge layer in said base region at an interface between said first semiconductor layer and said insulating layer.